5th Space Passive Component Days (SPCD), International Symposium

15-18 October 2024
ESA/ESTEC, Noordwijk, The Netherlands

Benjamin Nicolle(1) and Alexandre Moulin(1)

(1) Vishay SA
199 Boulevard de la Madeleine CS 71159
06003 Nice Cedex 1, France
Email:alexandre.moulin@vishay.com

INTRODUCTION

High frequency circuits are strongly anchored in the evolution of wireless technologies, offering a powerful way to send and receive data faster. The need for speed concerns communications in almost all markets - military, aerospace, automotive, and, obviously, mobile 5G. Passive components must comply with the physical specificities linked to these frequencies, and resistors are no exception. The "microwave" frequency range is 300 MHz to 300 GHz [1], but lumped resistors, while entering into this range, are more limited.

This paper describes ways to measure S-parameters and deduce impedance values of chip resistors at frequencies up to 70 GHz. A good board design alongside precise measurements allow to compare the impedance over frequency before and after AEC-Q200 tests and show the high stability of the CHA series of thin film chip resistors.

Precise measurements at high frequencies require suitable characterization boards ways of assembly and analyzing methods. Supplying these while demonstrating the impedance stability of Vishay resistors particularly in the demanding space environment, where electronic components must endure harsh conditions and continue to operate flawlessly is the primary objective of this application.

CHA SERIES RESISTOR

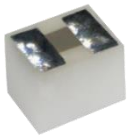

Fig. 1 – CHA02016

CHA series of microwave AEC-Q200 qualified resistors, available with gold and tin / silver terminations, offer best in class performance for mmWave, 5G, radar, and other high frequency applications. These miniaturized components are designed in such a way that their internal reactance is very small. When correctly mounted and used, they function as almost pure resistors on a very large range of frequencies up to 70 GHz. CHA series devices are available with ohmic values between 10 Ω and 500 Ω.

HIGH FREQUENCY RESISTOR MODEL

Parasitic elements inherent to resistors by construction are generated by the resistor-circuit interface.
Designers can use the S-parameters or impedance characterization to perform hyper-frequency simulations and compare system results. Component usage requires propagation into a PCB where the component is mounted as a quadripolar element. The mounting influence and design topology made with PCB technology permit high frequency characterization using calibration as required in hyper-frequency applications.
SMD component alone could be approach with an impedance Z. When the component is mounted on the board, the whole component including parasitic elements is modeled thanks to a π structure. (see Fig. 2).

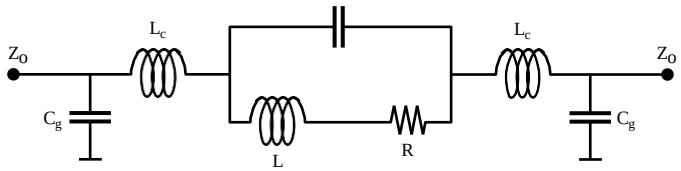

Fig. 2 - Electrical Model Equivalent for HF Applications of CH / CHA Component

Where:
- R is the nominal resistance value
- L is the inductance linked to the resistor
- C is the capacitance linked to the resistor
- Lc is the parasitic inductance due to the resistor mounting
- Cg is the parasitic capacitance due to the resistor mounting
- Zo is the characteristic impedance of the line

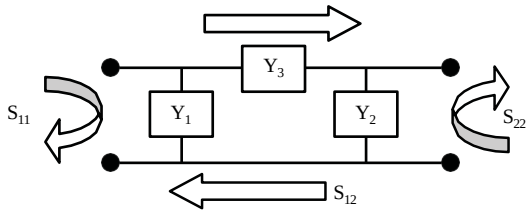

Fig. 3 - CHA quadripolar PI structure

The π structure illustrated in Fig. 3 is used as a two-port representation of the DUT. We derive impedance from the transmission admittance conversion (as well as ABCD parameters) form the measured S-parameters after calibration:

$$Z = B = \frac{-1}{Y_{21}} = Z_0 \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2.S_{21}}$$

Therefore, even if it is not possible to measure the impedance Z directly key component parameters, such as impedance and the influence of AEC-Q tests on impedance, can still be obtained.
As in the CH / CHA series datasheets, throughout this document we will use the normalized value |Z|/R, where R is the ohmic value of the resistor under test to visualize and compare the behavior of our CH / CHA component. Using this approach, Fig. 4 compares the normalized impedance over frequency of an ideal and real 50 Ω resistor.

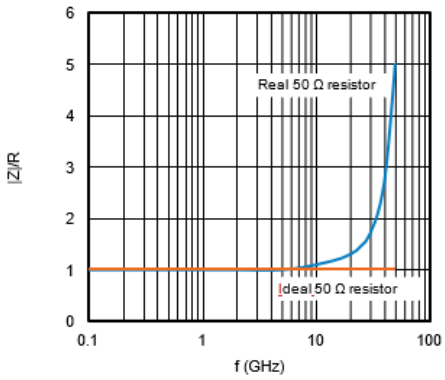

Fig. 4 - Comparing normalized impedance |Z|/R of ideal and real resistor

HIGH FREQUENCY PCB DESIGN

HF applications require high quality materials. Care should be taken to choose low loss substrates with adequate dielectric constant that can maintain its isolation properties to frequencies of 40 GHz and higher.
We design the 3D encrypted CHA component (substrate, ohmic value, termination etc). Using this 3D encrypted model, a top-down methodology permits to make the best compromise on the PCB (topology, characteristic impedance, connector layout etc) to enhance the CHA behavior after calibration during the measurements.
Finally, best choice (Fig. 5) is a specific PCB series with coplanar waveguide with ground (CPWG) topology for both thru reflect line (TRL) and device under test (DUT) boards.
The 3D HFSS encrypted components are available to customers.

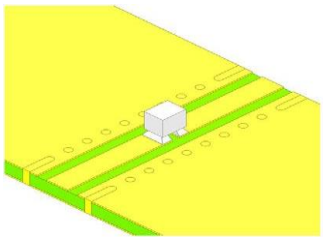

Fig. 5 - CHA mounted on DUT characterization board

To study the impact of AEC-Q200 tests on the DUT, we use HF connectors to allow easier mounting/unmounting during calibration and measurements regarding the sampling quantities. Using a TRL calibration instead of resistance-based calibration, the calibration cancels the effects of the VNA-cables-connectors-DUT over reference plan (Fig. 6).

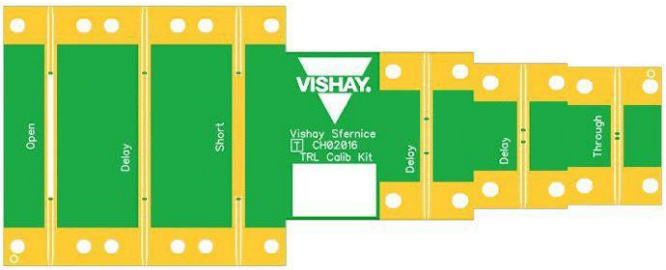

Fig. 6 - Thru reflect line calibration board

Via technology is used to avoid the substrate wave mode and increase the cut-off frequency in the pre-preg layer, maintaining a good impedance characteristic at 50 Ω in the 1 GHz to 70 GHz band. To be representative of customer applications and multi-layer stacking, especially for AEC-Q200 tests, we use a 1 mm multi-layer PCB as is standard in the industry. This avoids mechanical issues and permits easy electronic component assembly. A compromise between optimizing the impedance characteristic over frequency and minimizing discontinuities by the matching of the resistor footprint to the connector via tapered lines was found. This design is depicted in Figure 7

Fig. 7 - DUT characterization board

This was enabled by using a CPWG (Conductor-backed coplanar waveguide) as depicted in Figure 8, allowing for characterization up to 70 GHz with reference plans focused on the resistive layer.

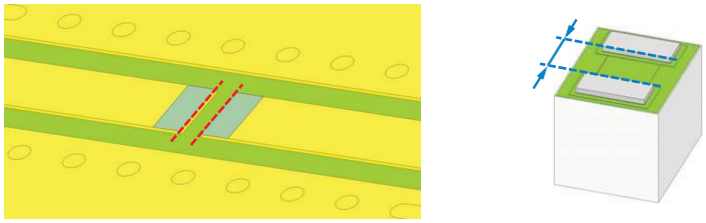

Fig. 8 - Reference plans for CHA characterization (red for DUT, blue for component)

MOUNTING

Due to the (very) small size of the 02016 package (approx. 0.4mm x 0.5 mm), the main assembly failure mode is excessive tilting (Fig. 9).

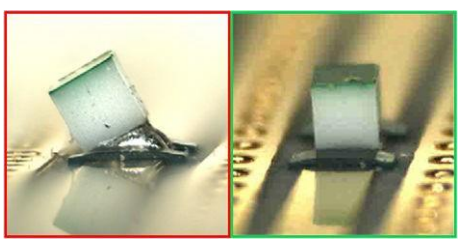

Fig. 9 - Excessive tilting vs. good assembly

To limit tilting during assembly and soldering, we recommend:
- to use the land pattern dimensions suggested in the CH / CHA datasheet,
- to deposit the right amount of solder paste by reducing the stencil thickness from 0.1mm down to 0.08 mm or by reducing the aperture size,
- to use the solder paste based on IPC-J-STD-005 (type 4 or higher) e.g. SAC 305 solder paste made of 96.5 % tin, 3 % silver, and 0.5 % copper for lead (Pb)-free soldering,
- to use the J-STD-020 thermal profile

By implementing these recommendations, the excessive tilting of the CHA 02016 case size can be reduced to a minimum.

AEC-Q200 COMPLIANT AND HYPER-FREQUENCY CHARACTERIZATION PROTOCOL

TABLE 1 - AEC-Q200 TEST PROCEDURES AND REQUIREMENTS

AEC-Q200 CLAUSE	TEST	PROCEDURE	GLOBAL PERFORMANCES	TYPICAL PERFORMANCES (25 Ω TO 250 Ω)
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 125 °C, unpowered	± 2 % ± 0.05 Ω	± 0.2 % ± 0.05 Ω
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	± 1.8 % ± 0.05 Ω	± 1.5 % ± 0.05 Ω
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power	± 2 % ± 0.05 Ω	± 0.75 % ± 0.05 Ω
8	Operational life	MIL-STD-202 method 108 condition D steady state T = 125 °C at rated power 90' on / 30' off / 1000 h	± 2.5 % ± 0.05 Ω	± 1 % ± 0.05 Ω
13	Mechanical shock	MIL-STD-202 method 213 condition C 100 *g*/6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	± 0.05 % ± 0.05 Ω	± 0.015 % ± 0.05 Ω
14	Vibration	MIL-STD-202 method 204 5 *g* for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
15	Resistance to soldering heat	MIL-STD-202 method 210 condition D Flux used: alpha 611 Solder temp.: 260 °C ± 5 °C Total immersion during 10 s	± 2.5 % ± 0.05 Ω	± 0.5 % ± 0.05 Ω
17	ESD	AEC-Q200-002	Classification 1C 1000 V_{DC} to 2000 V_{DC}	
18	Solderability	J-STD-002 - Preconditioning 4 h dry heat aging and 235 °C SnPb 5 s - 215 °C SnPb 5 s - 260 °C SnAgCu 10 s	Good tinning (≥ 95 % covered) No visible damage	
20	Flammability	UL 94	Class V-0 No burning	
21	Board flex	AEC-Q200-005	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C	

We applied all the AEC-Q200 tests on the component. In addition, we measured the high frequency stability before and after these selected tests:

- High temperature exposure: 1000 h at 125 °C unpowered
- Temperature cycling: 1000 cycles (-55 °C to +155 °C)
- Biased humidity: 1000 h at 85 °C / 85 % hum. and 10 % of operating power
- Operational life: 1000 h at rated power and Ta = 125 °C
-

S-parameter measurements and quadripolar impedance computation characterizations are made in real time thanks to the admittance conversion and computation capabilities of VNA, as presented in the “HF resistor summary” section above. The frequency characterization is summarized in Fig. 13 and Fig. 14.

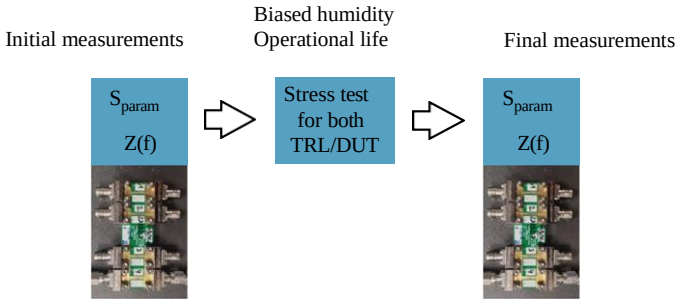

Fig. 13 - Serialization of measurements, comparison between final vs. initial measurements

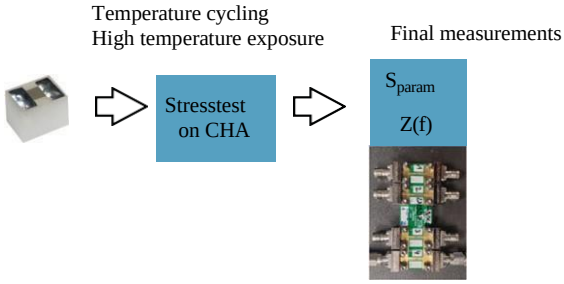

Fig. 14 - Comparison between final measurements vs. datasheet

HIGH FREQUENCY CHARACTERIZATION AND RESULTS

By using the test boards described in the previous sections, high accuracy values for the normalized impedance over frequency of the CHA series resistors were taken before and after being subjected to various AEC-Q200 test procedures. Fig. 15 shows the changes induced by exposure to the biased humidity test, Fig. 16 depicts changes originating from operational life testing, Fig. 17 shows the normalized impedance after high temperature exposure compared to datasheet values and finally Fig. 18 shows normalized impedance after temperature cycling alongside the datasheet value.

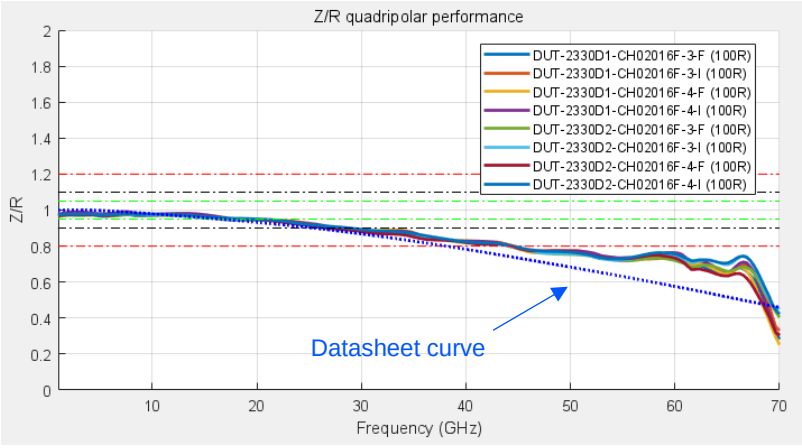

Fig. 15 - Frequency response of a 100 Ω; CHA02016 before (-I) and after (-F) a AEC-Q200 biased humidity test

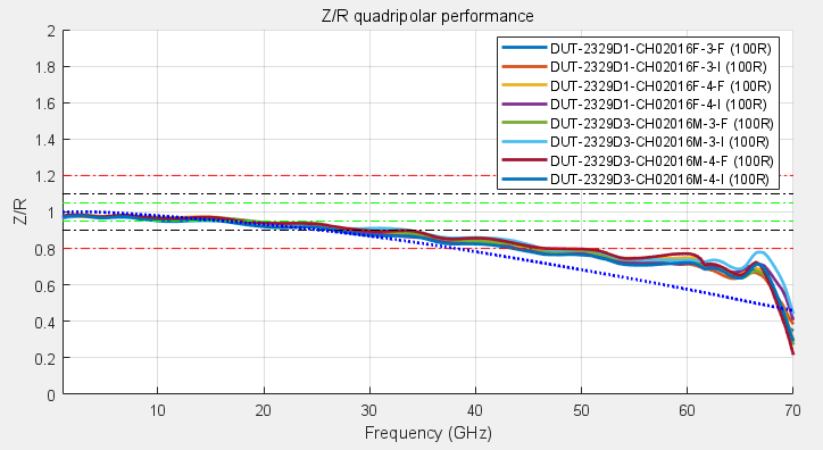

Fig. 16 - Frequency response of a 100 Ω; CHA02016 before (-I) and after (-F) a AEC-Q200 load life test

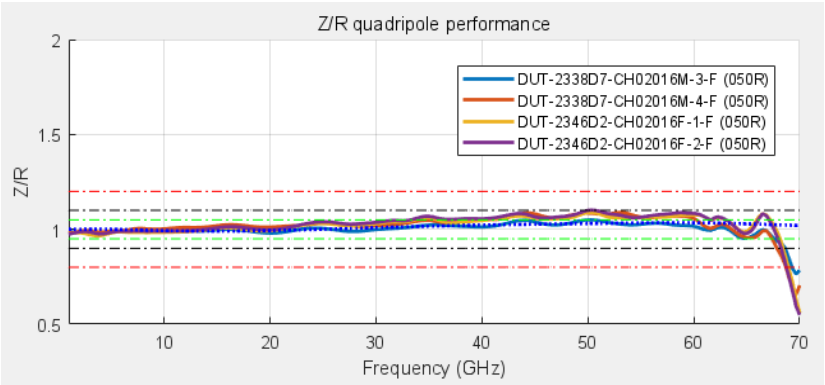

Fig. 17 - Frequency response of a 50 Ω; CHA02016 after AEC-Q200 temperature cycling vs. datasheet values

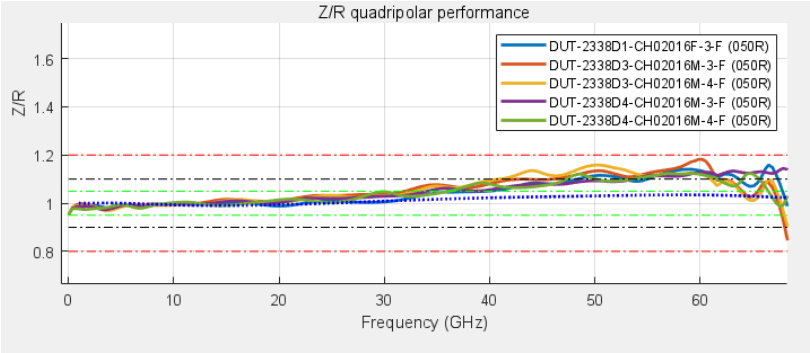

Fig. 18 – - Frequency response of a 50 Ω; CHA02016 after AEC-Q200 high temperature exposure vs. datasheet values

CHA02016 resistors provide stable high frequency performance up to 70 GHz, and maintain that stability even after the most stressful AEC-Q200 tests simulating harsh environmental conditions.